	Application No.	Applicant(s)
Notice of Allowability	10/053.870	TANI ET AL.
	Examiner	Art Unit
	Steven J. Mottola	2817
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to September 23 2003.		
2. The allowed claim(s) is/are <u>1-13 and 15-18</u> .		
3. The drawings filed on 24 January 2002 are accepted by the Examiner.		
 4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) ☐ All b) ☐ Some* c) ☐ None of the: 		
Certified copies of the priority documents have been received.		
2. Certified copies of the priority documents have been received in Application No		
3. Copies of the certified copies of the priority documents have been received in this national stage application from the		
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received: 5. Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).		
(a) ☐ The translation of the foreign language provisional application has been received.		
6. Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.		
or in the state of		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		
7. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.		
8. CORRECTED DRAWINGS must be submitted. (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached 1) hereto or 2) to Paper No		
(b) including changes required by the proposed drawing correction filed, which has been approved by the Examiner.		
(c) 🔲 including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No		
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.		
9. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s)		
1 ☐ Notice of References Cited (PTO-892) 3 ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 5 ☐ Information Disclosure Statements (PTO-1449), Paper No. 06 7 ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	4 ⊠ Interview Sul 6⊠ Examiner's A	ormal Patent Application (PTO-152) Immary (PTO-413), Paper No. 10603 Immendment/Comment Istatement of Reasons for Allowance Sieven J. Mortola Primary Examine:

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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or

additions be unacceptable to applicant, an amendment may be filed as provided by 37

CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than

the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr.

Brooks on October 9, 2003.

2. The application has been amended as follows: claim 18 has been rewritten in independent

form to include all of the limitations of canceled claim 14 and now reads as follows:

-- An operational amplifier, comprising:

a plurality of transistors including a transistor serving as a current source;

a bias generating circuit that applies a bias voltage to said transistor serving as a current

source; and

a bias voltage adjusting circuit that adjusts the bias voltage generated by said bias

generating circuit to change the current flowing through said transistor serving as a current

source,

wherein said bias voltage adjusting circuit comprises a plurality of switches for adjusting

the bias voltage among a plurality of values.--

jévén J. Mottola

fimary Examiner